

A Novel Audio/Video Decoder for Video Recorders

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Abstract - This paper describes an integrated audio/video decoder for video recorders. The IC has a number of novel features designed to improve video decoder performance over what is now available in the market whilst also introducing measures to reduce the implementation cost and the power consumption.

I. INTRODUCTION

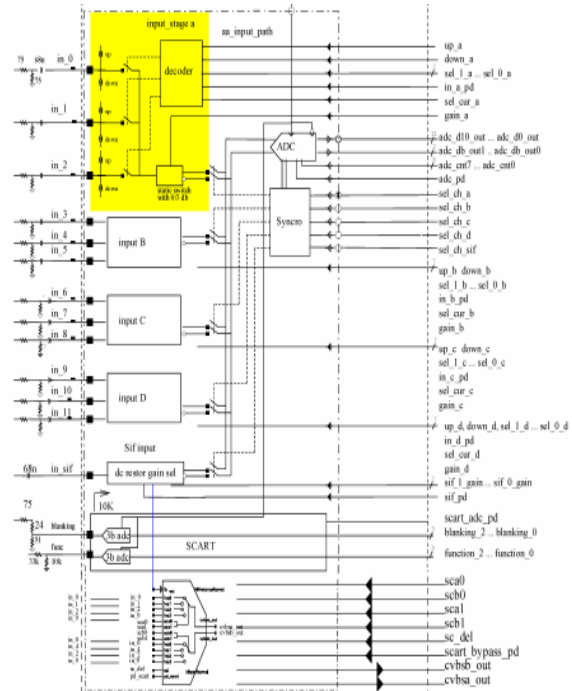
It may seem anomalous to introduce an analogue video decoder IC when all the talk is of analogue transmission switch off and digital broadcasting. Also most major semiconductor manufacturers already have in the market an I.C. that performs this function. However for legacy reasons and because of the increase in demand from markets that have later dates for analogue switch-off, (e.g. East Europe, India and South America), it is likely that analogue decoding will be a requirement well into the next decade, (indeed most hard disc recorders now require two such I.C.s). It was therefore decided, to have a fresh look at this function and see where cost savings could be made whilst also improving the decoder performance. Quality improvements include a ‘memory-less’ 3D comb architecture, a bandwidth improvement for video cassette recordings and an automatic YC delay compensation.

The basic function of the AV decoder is to accept video inputs in a variety of formats, (CVBS/YPbPr/RGB), and standards, (NTSC/PAL/SECAM), and to digitize, decode and format them into a digital format, usually BT656, for the MPEG codec. In addition it is also desirable to integrate an audio decoder for decoding of the sound IF signal (SIF) into baseband audio. Again multiple standards should be accepted – NICAM, EIA-J, BTSC etc.

II. ANALOGUE INTERFACE

The requirement to interface to a variety of different inputs and to digitize these with sufficient quality puts a lot of demand on the analogue front end circuitry and usually these result in a lot of area and power consumption being used. It was decided in this design to implement as much of the analogue functionality as possible in the digital domain to circumvent this. A simplified block diagram of the analogue front end is shown in Figure 1. The I.C. can accept up to 12 inputs, 4 of which can be digitized simultaneously, (inputs A-D in Fig.1); this allows almost all use cases to be accommodated without the need for external multiplexing devices. The inputs are AC coupled so the required level shifting for the ADC is provided by simple push-pull current sources which are controlled from the digital circuitry, (signal up/down in Fig. 1). Also a single delta-sigma 11 bit ADC is

used with the four selected inputs being analogue multiplexed at 4 times the sample frequency; this approach significantly reduces the operating power consumption and the area of the analogue circuitry. In addition independent loop-through of two of the composite video inputs is provided, a European SCART requirement, again to reduce external component cost.



notch or a low pass filter. The choice of which mode to operate in is done by evaluating the error produced from each mode simultaneously and choosing that with the lowest error. The error evaluation is done for both the chrominance and luminance signals ensuring the output is as free from artifacts as possible under all signal conditions.

IV. SAMPLING STRATEGY

After some initial experiments with FPGAs, it was decided to isolate the sampling of the video and audio decoders to prevent sub-multiple clock frequencies within the baseband audio bandwidth entering the audio SIF decoder. It was chosen to clock the ADC and the audio decoder at a free-running 24.576MHz, (with the ADC running at 4x that frequency). However the BT656 output is required to run at 27MHz so a sample rate converter (SRC) is used to convert between the two sample domains. The SRC also fulfills the function of decimating and filtering the input video. Further a filtered, lower jitter, version of the line-locked 27MHz is also provided. The output decoded video is fed into a FIFO memory with the crude 27MHz clock, and clocked out with the ‘cleaned up’ version of the clock. This helps ensure signals with a lot of noise or non-compliant signals such as VCR inputs do not cause excessive jitter on the BT656 output.

V. DECODING OF VCR VIDEO

Video Cassette Recorders use a technique known as color-under for recording. The luminance information is FM modulated onto a carrier of approximately 3.5MHz, whereas the chrominance information, (and also the luminance information contained within it), is re-modulated onto a lower frequency carrier (approximately 600 kHz) to avoid problems recording at higher frequencies. Because of this re-modulation of the chrominance component onto another carrier the phase relationship with the original sub-carrier is lost. Without this phase relationship it is no longer possible to comb the higher frequency component to separate the luminance and chrominance, with the result that the higher frequency luminance is discarded. However, by adopting the architecture shown in Figure 2, the high frequency luminance can be added into the low pass luminance using a different phase of the sub-carrier. When the HF luminance is re-modulated with the original phase relationship original waveform is reconstructed with a higher bandwidth.

The phase of the second re-modulator is adjusted based on information derived from a high pass filter. The correct phase for the addition of the luminance signals is found by detecting the improved sharpness of the luminance signal for a certain sub-carrier phase. This can be done with a high pass filter, a square law function, (to rectify the high pass filter output and increase the weighting given to slope of the signals), and an accumulator to measure the amount of edge detail in the image. The adjustment of the correct phase is done as an iterative process, (but the phase does not change quickly so this is satisfactory). The additional phase offset is added into the sub-carrier phase derived from the input signal.

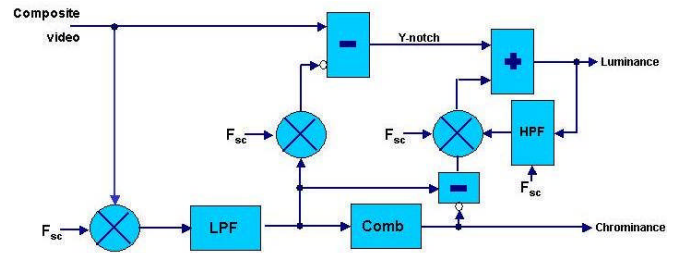


Fig. 1 Improved VCR decoding

VI. YC DELAY COMPENSATION

It is not uncommon for the chrominance and luminance components of the video to not be co-timed. The non-timed signals further ‘spread’ the edges of the video and result in a very soft, apparently blurred image. Although most current decoders provide a manual control to allow the signals to be retimed, to do on real signals, which have a varying delay, is clearly impossible. It was therefore decided to incorporate an automatic compensation in this design. The edge content of the chrominance and luminance components is extracted and a correlation function is calculated for various delay settings. A curve fit is then run to determine the best correlation and this delay setting is then applied.

VII. POWER STRATEGY

Low power consumption is a given in today’s consumer equipment and in this respect decisions made in the design process, (e.g. for a single delta-sigma ADC and other strategies), mean the active power consumption of the final IC is not expected to exceed 450mW. In addition when the video recorder is put into standby mode the IC may be ‘powered down’ whereby all of the IC is run at a much reduced clock rate, thereby retaining all register values and the analogue loop-through function, whilst also being able to be ‘woken up’ as required. Standby power consumption is less than 10mW.

VIII. EXPERIMENTAL RESULTS

A test IC was produced to allow the evaluation of the analogue front end and the video decoder and performed as expected from simulation. The bandwidth improvement for recordings of video cassettes is more than 0.5MHz. Some further improvements were made as result of testing on ‘real’ signals and the production I.C. is now in fabrication.

IX. CONCLUSIONS

This paper has discussed a number of improvements that can be made to an old warhorse, the analogue video decoder. Analogue video will remain a requirement on video recorders for the foreseeable future. This paper shows that there are still further measures that may be implemented that can improve the resulting recorded image, whilst also saving on the cost and power requirements.